**ECE 571**

**Design and Verification**

**DDR4 Memory Controller Interface**

**by**

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1. **Scope**

This document provides details of planning, design, and verification of DDR4 Controller Interface for ECE517 Final Project.

* 1. **Functional Overview**

The main purpose of the final project is design and test DDR4 Controller using System Verilog constructs. The project is developed under Prof. Faust’s guidance and uses the lecture on TLM as an example. The project breaks into three major blocks: the synthesizable interface, which provides the methods to translate the commands, data into pin signal levels used by DDR Controller and Memory DDR4 DIMM. The second block is DDR Controller, which is built as a behavior model and iterative convert to synthesizable block as the example in TLM lecture. The last block is DIMM model and other parts, which used in test bench to verify the DDR Interface.

1. **Definition**

tCCD CAS to CAS latency

tRRD Activate to Activate latency

tWRT Write to Read delay

tRTP Read to PreCharge.

tWR Write to PreCharge

tRCD Activate to CAS latency

Trp PreCharge to ACT latency

tCL CAS to DQ read

tCWL CAS to DQ write

tZQ Initialize process to ACT

AL Additive Latency

Burst Length Number of Bytes Read/Write

Preamble 1 or 2nCK

REF Refresh period